MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2017/2018

DET5058 – DIGITAL ELECTRONICS
(DEE)

9 March 2018
3.00pm – 5.00pm
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This question paper consists of **6** pages (**5** pages with **4** questions and **1** page for appendix).
2. Answer **ALL** questions. All necessary working steps must be shown.
3. Write all your answers in the answer booklet provided.

QUESTION 1 [25 Marks]

a) Provide **FOUR** analog quantities that are normally converted into digital signals.

[4 marks]

b) Name the **FOUR** component that completes a computer system.

[4 marks]

c) One of the advantage of digital systems over analog systems is "digital systems are less affected by noise". Explain why.

[2 marks]

d) Convert the BCD number 001101111000011000 01 into:

(i) Decimal
(ii) Binary
(iii) Octal
(iv) Hexadecimal
(v) Gray

[10 marks]

e) Given 10001111_2 and 11110011_2 are both in 2's complement form.

(i) Add the numbers in 8-bit 2's complement form.

[2 marks]

(ii) State whether overflow occurred or not. Support your statement through redoing the addition in decimal and evaluating the addition result.

[3 marks]

Continued...

QUESTION 2 [40 Marks]

Given a Boolean expression $X = \overline{\overline{A\overline{B}C} \cdot \overline{A\overline{B}}} + \overline{\overline{BC} \cdot \overline{B\overline{C}D}}$, solve the following questions.

a) Draw the logic diagram of the Boolean expression.

[7 marks]

b) Prove that the expression can be reduced to $X = A\overline{B} + BC + BD$ by using rules of Boolean algebra.

[8 marks]

c) Provide the truth table for the Boolean expression.

[5 marks]

d) Based on the provided truth table, provide the standard SOP expression in terms of algebraic function.

[3 marks]

e) Assuming don't care condition exist, where $d(A, B, C, D) = \sum m(0, 1, 2, 3)$, state whether the Boolean expression can be further reduced as compared to reduced expression in (b). You may apply Karnaugh map to prove your statement.

[7 marks]

f) Implement the reduced Boolean expression in (e) using NAND gates only.

[4 marks]

g) Draw the output waveform for the output expression based on the given input waveforms in Figure 1. Ignore don't care conditions introduced in question (e).

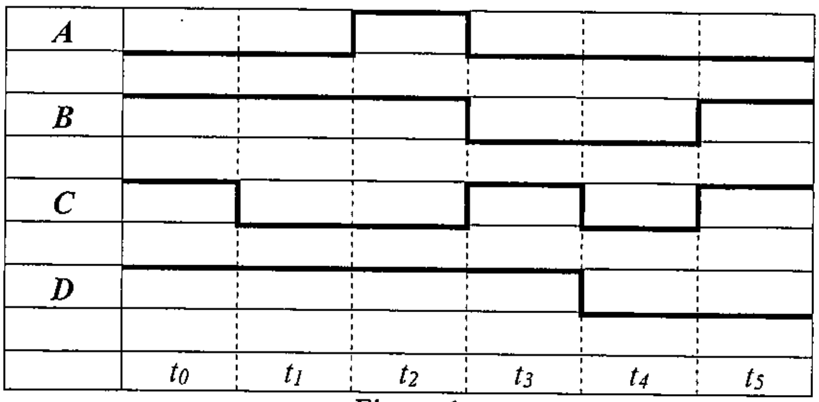

Figure 1

[6 marks]

Continued...

QUESTION 3 [20 Marks]

a) Complete the truth table representing full subtractor below. Note that, $A - B = D$.

B_{in}	A	B	B_{out}	D
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[8 marks]

b) Name the combinational logic represented by the circuit diagram in Figure 2, and produce the output expression for the combinational logic.

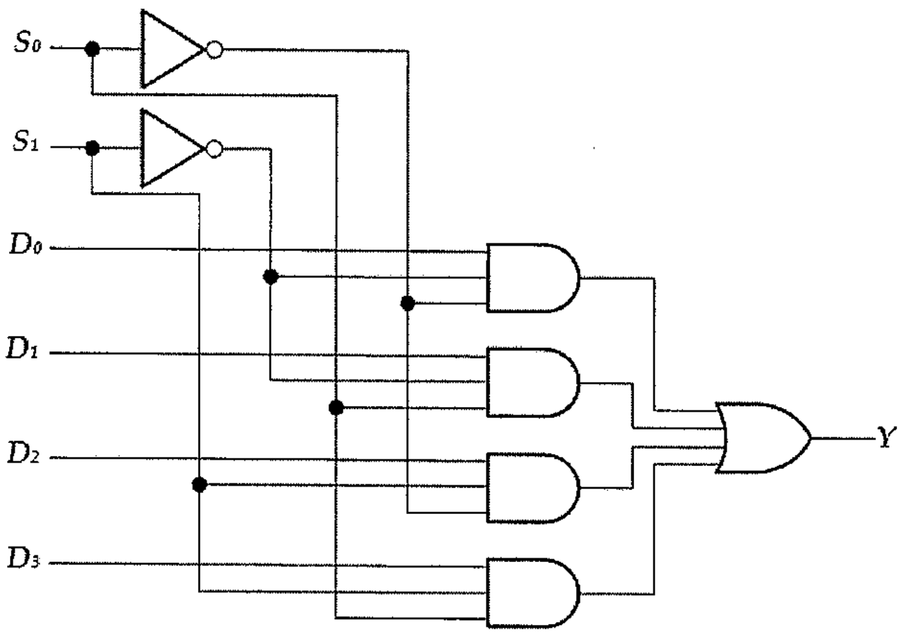

Figure 2

[5 marks]

Continued...

QUESTION 3 (Continued)

c) Based on your answer in (b), draw the output waveform Y, based on the given input waveforms in Figure 3.

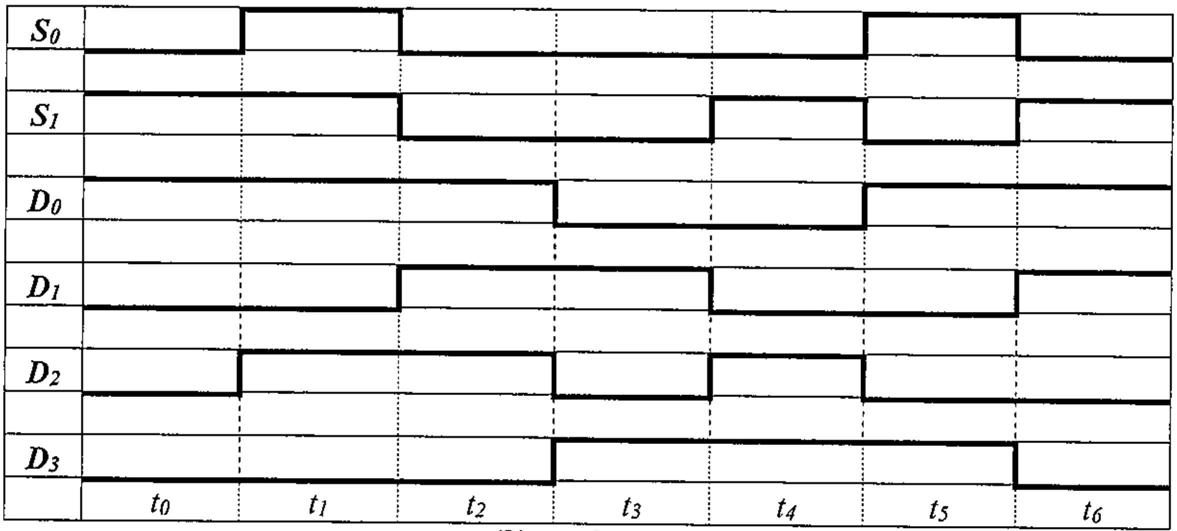

Figure 3

[7 marks]

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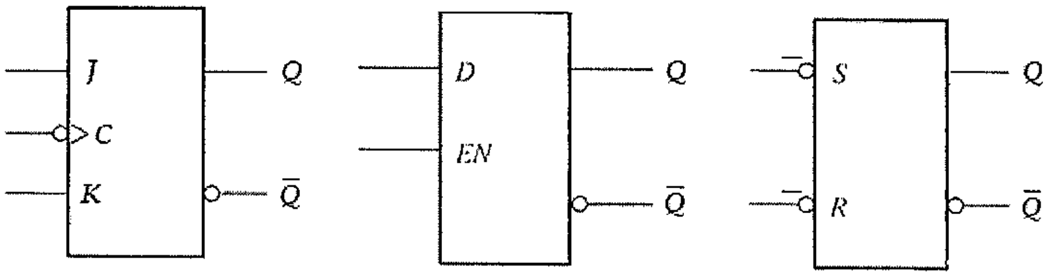
QUESTION 4 [15 Marks]

a) Name the latches/flip-flops represented by the logic symbol in Figure 4.



(i) (ii) (iii)

Figure 4

[6 marks]

b) If the latches/flip-flops in Figure 4 is arranged as in Figure 5, draw the output waveforms of Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$ and Q_3, $\overline{Q}_3$, based on the given input waveforms in Figure 6. Assume all latches/flip-flops are initially LOW.

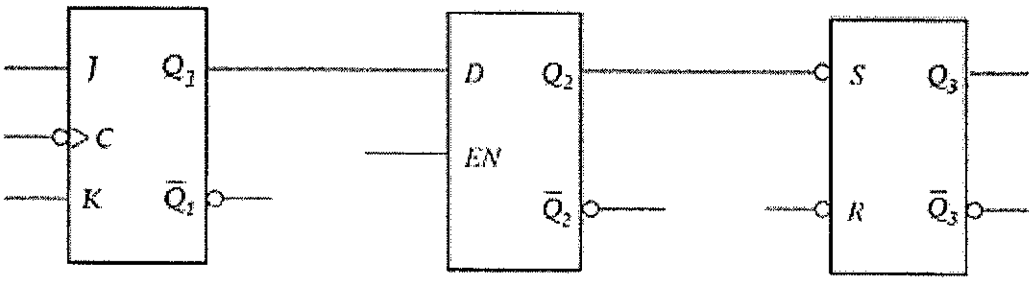


Figure 5

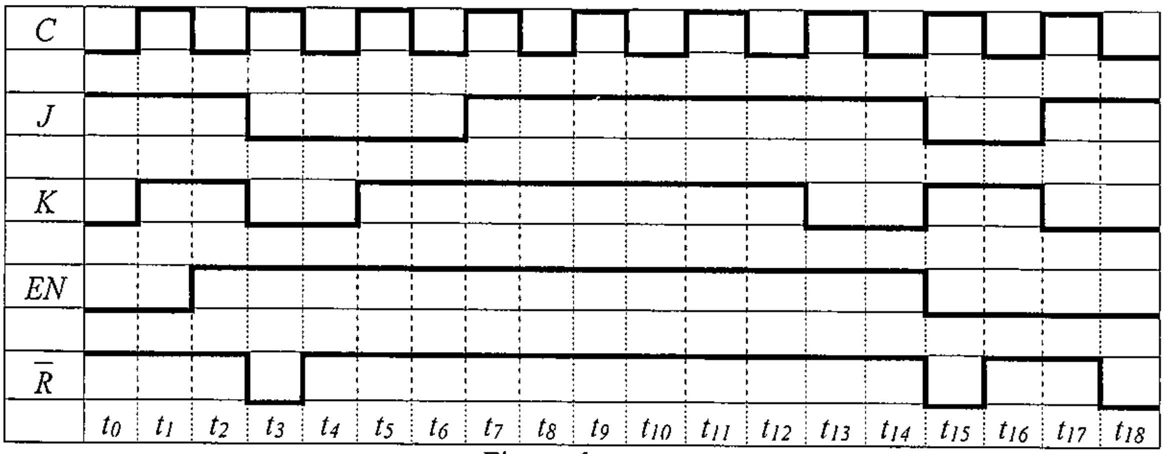


Figure 6

[9 marks]

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APPENDIX: RULES OF BOOLEAN ALGEBRA

1. $A + 0 = A$
2. $A + 1 = 1$
3. $A \cdot 0 = 0$
4. $A \cdot 1 = A$
5. $A + A = A$
6. $A + \overline{A} = 1$
7. $A \cdot A = A$
8. $A \cdot \overline{A} = 0$
9. $\overline{\overline{A}} = A$
10. $A + AB = A$
11. $A + \overline{A}B = A + B$
12. $(A + B)(A + C) = A + BC$